REMARKS

Claims 1-9 are pending in the present application. Claims 8 and 9 were indicated as allowed, and claims 2-7 were indicated as being allowable if amended to include the limitations of independent claim 1. Applicants appreciate the indications of allowable subject matter, but respectfully request reconsideration of the rejection of claim 1 as discussed in detail below.

In addition to amendments to rejected claim 1, please note that allowable claims 2-9 have been amended herein. The amendments to claims 2-9 do not narrow the scope of the claims and are not made for reasons related to patentability. However, it is submitted that claims 2-9 should remain allowable for the same reasons indicated by the Examiner in the outstanding Office Action.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Matsui (US 5,982,050). This rejection is traversed and thus reconsideration is requested in view of the following remarks.

Claim 1 recites a capacitor device, comprising: a plurality of electric double-layer capacitors connected in series; and a plurality of balance resistor portions each comprising m resistors connected in parallel with each other and having equivalent resistance to each other, m being an integer greater than or equal to two; the plural balance resistor portions being connected in parallel to the plural electric double-layer capacitors, respectively.

The Examiner stated that Matsui discloses a balance resistor portion in which m (which is an integer of two or above) resistors having an equivalent resistance are connected in parallel (106, 108). However, as it is clear from the disclosures of Matsui, e.g., column 2, lines 4-10, and the depiction in FIG. 2, the balance resistors 106 and the resistors 108 constituting the balance transistor portion are not respectively connected in parallel. Matsui does not disclose a plurality of balance resistor portions each comprising plural resistors connected in parallel or that such plural balance resistor portions are connected in parallel to the plural electric double-layer capacitors, respectively, as recited in claim 1. Further, if the Examiner is relying on the resistors 106 and 108 as the plural (i.e., m) resistors, such an interpretation does not meet the claim language because the resistors 106 and 108 cannot be said to be in parallel with each other and at the same time form a balance resistor portion that is in parallel with a capacitor 100. Moreover,

Matsui does not disclose that the resistance of the resistor 108 is equivalent to the resistance of the balance resistor 106 and thus does not meet the claimed limitation of m resistors having equivalent resistance to each other.

On the other hand, according to the "balance transistor portion" recited in claim 1, m (which is an integer of two or above) resistors having an equivalent resistance are connected in parallel (see e.g., FIG. 1 of the present application) to each other, and each balance resistor portion comprising the m resistors is connected in parallel with a capacitor.

According to the balance transistor portion shown in FIG. 2 of Matsui, the balance resistor 106 and the resistor 108 are not connected in parallel with each other. Therefore, if any one of the balance resistor 106 and the resistor 108 is broken and becomes open, a resistor is omitted from a single cell 100 connected to the broken resistor. Accordingly, the voltage applied to the single cell 100 rises drastically, so that each single cell 100 cannot be charged in a balanced manner.

On the other hand, claim 1 recites that each balance resistor portion, which is connected in parallel to a capacitor, comprises a plurality of resistors connected in parallel to each other. Therefore, even if any of the resistors is broken, a resistor connected in parallel with the capacitor is still present. Accordingly, the voltage applied to the electric double-layer capacitor does not rise drastically, so that each double-layer capacitor can be charged in a balanced manner.

Because of the distinctions discussed above, claim 1 is not anticipated by Matsui. Moreover, no obvious modification of Matsui would result in or otherwise render obvious the invention of claim 1. Accordingly, it is submitted that claim 1 is allowable over the prior art of record.

In view of the above, it is submitted that the present application is in condition for allowance. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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